WHAT IS CLAIMED IS:

1. A signal bounce inhibiting device for preventing from power/ground bounce, comprising:

an electric level toggling circuit receiving a first internal signal of a first chip, and toggling said first internal signal into a first output signal in response to a first toggling control signal inputted therein; and

an electric level recovering circuit receiving said first output signal, and recovering said first output signal into said first internal signal required by a second chip in response to a first recovering control signal inputted therein.

2. The signal bounce inhibiting device according to claim 1 wherein said electric level toggling circuit is disposed in an output stage of said first chip and said electric level recovering circuit is disposed in an input stage of said second chip.

3. The signal bounce inhibiting device according to claim 1 wherein said electric level toggling circuit further receives a second internal signal and remains said second internal signal unchanged as a second output signal in response to a second toggling control signal inputted therein, and said electric level recovering circuit remains said second output signal unchanged in response to a second recovering control signal inputted therein so as to provide said second internal signal for said second chip.

4. The signal bounce inhibiting device according to claim 3 wherein said electric level toggling circuit includes a first count of electric level toggling units for toggling a second count of said first internal signals into said first output signals in response to said second count of first toggling control signals, and remaining a third count of said second internal signals into said second output signals in response to said third count of second toggling control signals.

5. The signal bounce inhibiting device according to claim 4 wherein said electric level recovering circuit includes said first count of electric level recovering units for recovering said second count of said first output signals into said first internal signals in response to said second count of said first recovering control signals, and remaining said third count of said second output signals into said second internal signals in response to said third count of said second recovering control signals.

6. The signal bounce inhibiting device according to claim 3 wherein said electric level toggling circuit includes a plurality of electric level toggling units, each of which includes:

a register for inputting therein and storing a certain toggling control signal; and

an XOR gate for receiving said certain toggling control signal and a certain internal signal to perform a first XOR operation, thereby toggling said certain internal signal or remaining said certain internal signal unchanged so as to obtain a certain output signal.

7. The signal bounce inhibiting device according to claim 6 wherein said electric level recovering circuit includes a plurality of electric level recovering units, each of which includes:

a register for inputting therein and storing a certain recovering control signal corresponding to said certain toggling control signal; and

an XOR gate for receiving said certain recovering control signal and said certain output signal to perform a second XOR operation, thereby toggling or remaining said certain output signal so as to recover said certain output signal into said certain internal signal.

8. The signal bounce inhibiting device according to claim 7 wherein said first and said second toggling control signals are identical to said first and said second recovering control signals.

9. A method for providing internal signals from a first chip to a second chip with inhibited power/ground bounce, comprising steps of:

asserting a plurality of toggling control signals including a first count of first toggling control signals and a second count of second toggling control signals;

toggling said first count of said internal signals into said first count of output signals in response to said first count of said first toggling control signals, and remaining said second count of said internal signals unchanged in response to said second count of said second toggling control signals;

asserting a plurality of recovering control signals correlating to said plurality of toggling control signals, and including said first count of first recovering control signals and said second count of second recovering control signals; and

recovering said first count of said output signals into said first count of said internal signals in response to said first count of said first recovering control signals, and remaining said second count of said internal signals unchanged in response to said second count of said second recovering control signals.

10. The method according to claim 9 wherein said first and said second toggling control signals are identical to said first and said second recovering control signals.

11. The method according to claim 9 wherein said first toggling control signal and said first recovering control signal are both at high levels, and said second

toggling control signal and said second recovering control signal are both at low levels.

12. A signal bounce inhibiting device embedded in an integrated chip for preventing signals from power/ground bounce, comprising:

an electric level toggling circuit toggling a first internal signal into a first output signal in response to a first toggling control signal and remaining a second internal signal unchanged as a second output signal in response to a second toggling control signal; and

a storing device for storing said first toggling control signal and said second toggling control signal.

13. The signal bounce inhibiting device according to claim 12 wherein said electric level toggling circuit includes a first count of electric level toggling units for toggling a second count of said first internal signals into said first output signals in response to said second count of first toggling control signals, and remaining a third count of said second internal signals into said second output signals in response to said third count of second toggling control signals.

14. The signal bounce inhibiting device according to claim 12 wherein said electric level toggling circuit includes a plurality of electric level toggling units, each of which includes an XOR gate for receiving said first toggling control signal and said first internal signal to perform a first XOR operation, thereby toggling said first internal signal, or for receiving said second toggling control signal and said second internal signal to perform a second XOR operation, thereby remaining said second internal signal unchanged.

15. The signal bounce inhibiting device according to claim 12 wherein said storing device includes a plurality of storing units, each of which includes a

register for inputting thereinto and storing said first toggling control signal or said second toggling control signal.

16. The signal bounce inhibiting device according to claim 12 further comprising an electric level recovering circuit disposed in a target chip for receiving and recovering said first output signal into said first internal signal in response to a first recovering control signal inputted therein.

17. The signal bounce inhibiting device according to claim 16 wherein said electric level recovering circuit remains said second output signal unchanged in response to a second recovering control signal so as to provide said second internal signal for said target chip.

18. The signal bounce inhibiting device according to claim 16 wherein said electric level recovering circuit includes a first count of electric level recovering units for recovering a second count of said first output signals into said first internal signals in response to said second count of said first recovering control signals, and remaining said third count of said second output signals into said second internal signals in response to said third count of said second recovering control signals.

19. The signal bounce inhibiting device according to claim 16 wherein said electric level toggling circuit includes a plurality of electric level toggling units, each of which includes an XOR gate for receiving said first toggling control signal and said first internal signal to perform a first XOR operation, thereby recovering said first internal signal in said target chip, or for remaining said second internal signal unchanged so as to obtain a second output signal.

20. The signal bounce inhibiting device according to claim 16 wherein said electric level toggling circuit includes a plurality of storing units, each of

which includes a register for inputting therein and storing said first recovering control signal or said second recovering control signal.